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II. CLAIM AMENDMENTS

1. (Cancelled)

2. (Currently Amended) The communication device of ~~Claim 1~~claim 20, wherein the signal acquisition component comprises a hardware initial synchronization block which has at least one of reprogrammable parameters and reprogrammable algorithms.

3. (Currently Amended) The communication device of ~~Claim 1~~claim 20, wherein the processor controls at least one of the first RAM and the first registers, and the second RAM and the second registers.

4. (Currently Amended) The communication device of ~~Claim 1~~claim 20. wherein the W-CDMA transmitter comprises a first programmable pulse shaping filter, and wherein the receiver comprises a second programmable pulse shaping filter.

5. (Original) The communication device of Claim 4, wherein the first pulse shaping filter and the second pulse shaping filter are programmable to perform GMSK filtering, and wherein the transmitter and receiver are configured to interface with a GSM front-end.

6. (Original) The communication device of Claim 5, wherein the processor performs a protocol in accordance with a GSM protocol stack.

7. (Currently Amended) The communication device of ~~Claim 1~~claim 20, wherein the processor, the transmitter and the receiver are configured for waveform processing of signals in accordance with a predetermined format, wherein the predetermined format is one of the following: UMTS, Satellite UMTS, Galileo, GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and ARIB.

8. (Currently Amended) The communication device of ~~Claim 1~~claim 20, wherein the transmitter comprises at least one element which is one of the following: synchronization hardware to slave transmit start epochs to events external to the

transmitter; a burst generator for realizing discontinuous transmissions; a quadrature pseudo-noise (QPN) channel containing one or more spreaders with a predetermined amplification of an output signal; a combiner to accumulate the QPN channel output signal; a PN code generator; a scrambling code generator; a scrambler; a combiner which accumulates a scrambling code output; a pulse shaping oversampling filter; and an NCO and upconverter for carrier precompensation.

9. (Original) The communication device of Claim 8, wherein the PN code generator is configured as a RAM in which PN codes are downloaded under control of the processor.

10. (Original) The communication device of Claim 8, wherein the scrambling code generator is configured as a programmable Gold Code generator.

11. (Original) The communication device of Claim 8, wherein the QPN channel is configured to execute UMTS forward or return link transmission.

12. (Original) The communication device of Claim 8, wherein an amplification of the spreader output is configured to perform a transmit power control.

13. (Currently Amended) The communication device of ~~Claim 1~~claim 20, wherein the transmitter comprises a time interpolator to perform sub-chip time alignments.

14. (Currently Amended) The communication device of ~~Claim 1~~claim 20, wherein the transmitter is configured for multi-code transmission.

15. (Canceled).

16. (Currently Amended) The communication device of ~~Claim 36~~claim 20 wherein the receiver further comprises a downconverter connected to an input of the pulse shaping filter so as to interface at a front-end at an intermediate frequency.

17. (Currently Amended) The communication device of ~~Claim 36~~claim 20 wherein the receiver is configured to execute forward link and return link waveforms in

accordance with a predetermined format, wherein the predetermined format is one of the following: UMTS, Satellite UMTS, Galileo, GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and ARIB.

18. (Currently amended) A communication device for wideband code division multiple access (W-CDMA) signal transmission and reception, comprising:

a W-CDMA transmitter comprising at least one of a first RAM and first registers arranged to store first parameters so as to configure the transmitter's operation;

a W-CDMA receiver comprising at least one of a second RAM and second registers arranged to store second parameters so as to configure the receiver's operation;

a signal acquisition component; and

a processor in data communication with the W-CDMA transmitter, the W-CDMA receiver and the signal acquisition component, wherein the processor is configured to provide for software configuration of the first and second parameters;

wherein the receiver comprises:

a pulse shaping filter;

a level control block configured to receive an output from the pulse shaping filter;

a demodulator configured to receive an output from the level control block and track multi-path components received from a base station; and

a reference demodulator configured to receive the output from the level control block and configured to estimate noise;

~~The communication device of Claim 36~~ wherein the level control block comprises:

a programmable shifter configured to receive an input from the pulse shaping filter and to perform coarse grain dynamic control;

a programmable multiplier configured to receive an input from the shifter and to perform fine grain dynamic control;

a first overflow counter configured to receive an input from the multiplier and to operate on a most significant bit and a second most significant bit;

a second overflow counter configured to receive an input from the multiplier and to operate on the second most significant bit and a third most significant bit; and

a saturation logic configured to receive an input from the multiplier and to operate to limit the input received from the multiplier.

19. (Currently Amended) The communication device of ~~Claim 36~~claim 20 wherein the level control block is included in a runtime control ioop controlled by the processor.

20. (Currently amended) A communication device for wideband code division multiple access (W-CDMA) signal transmission and reception, comprising:

a W-CDMA transmitter comprising at least one of a first RAM and first registers arranged to store first parameters so as to configure the transmitter's operation;

a W-CDMA receiver comprising at least one of a second RAM and second registers arranged to store second parameters so as to configure the receiver's operation;

a signal acquisition component; and

a processor in data communication with the W-CDMA transmitter, the W-CDMA receiver and the signal acquisition component, wherein the processor is configured to provide for software configuration of the first and second parameters;

wherein the receiver comprises:

a pulse shaping filter;

a level control block configured to receive an output from the pulse shaping filter;

a demodulator configured to receive an output from the level control block and track multi-path components received from a base station; and

a reference demodulator configured to receive the output from the level control block and configured to estimate noise;

~~The communication device of Claim 36~~ wherein the demodulator comprises:

a Rake filter producing a signal at a chip rate which is a coherent accumulation of channel corrected multipath components resulting from one base station; and

a tracking unit using the signal at the chip rate for descrambling and despreading a plurality of waveform channels,

wherein the Rake filter comprises:

a FIFO to buffer samples at the chip rate coming from the level control block;

a delay line containing a plurality of registers, an input of the delay line being connected to an output of the FIFO;

a plurality of finger blocks, inputs of the finger blocks being connected to programmable tap positions on the delay line; and

a summer of complex outputs of the finger blocks at a chip rate.

21. (Original) The communication device of Claim 20, wherein the finger blocks are respectively grouped in a first multipath group and a second multipath group, the Rake filter being configured to accumulate energies of the outputs of the first multipath group and the second multipath group, and to use the accumulated values to feed a time error detector of the a DLL used for time tracking.

22. (Original) The communication device of Claim 20, wherein the Rake filter comprises memories to hold at least one of a spreading code for a channel correction pilot, a scrambling code for a channel correction pilot, a channel correction pilot symbol modulation, and a channel correction pilot symbol activities.

23. (Original) The communication device of Claim 22, wherein the memories are controlled by the processor.

24. (Original) The communication device of Claim 22, wherein the finger block comprises:

a channel correction pilot descrambler;

a channel correction pilot despreader connected to an output of the channel correction pilot descrambler;

a channel correction pilot filter connected to an output of the channel correction pilot despreader and performing a coherent channel correction pilot symbol accumulation over a programmable number of steps, and producing a weighted average on a programmable number of the coherent channel correction pilot symbol accumulation over a programmable number of steps;

a channel estimator connected to the channel correction pilot filter and generating a channel estimation at the chip rate and using outputs of the pilot filter;

a channel corrector connected to the channel estimator and performing a multiplication of an incoming stream with a complex conjugate of the channel estimation;

a calculator connected to the pilot filter and configured to calculate a slot energy;

a comparator connected to the calculator and configured to compare the slot energy with a programmable threshold; and

a circuit connected to the comparator and configured to force the channel estimation to zero if the threshold is not exceeded.

25. (Original) The communication device of Claim 24, wherein the finger is configured for slow and fast fading compensation by programming the channel correction pilot filter for slow fading, the channel correction pilot filter performing a coherent accumulation over a slot, and performing a weighted average over previous-previous, previous, actual and next obtained slot values yielding a channel estimation per slot, which is applied by the channel corrector; and for fast fading, the channel correction pilot filter performing a coherent accumulation over a slot, and then deriving channel estimations through interpolating consecutive the coherent accumulations over a slot, yielding channel estimations with sub-symbol timing, which are applied by the channel corrector.

26. (Currently Amended) The communication device of ~~Claim 36~~claim 20 wherein the reference demodulator comprises an accumulator of programmable length of absolute values of samples at a chip rate, and a low pass filter operating on the accumulator output.

27. (Currently Amended) The communication device of ~~Claim 36~~claim 20 wherein the reference demodulator is included in a runtime control loop controlled by the processor.

28. (Currently Amended) The communication device of ~~Claim 36~~claim 20 wherein the demodulator is configured to perform satellite diversity.

29. (Currently Amended) The communication device of ~~Claim 1~~claim 20, wherein the device is configured to perform ranging measurements to geostationary satellites.

30.-34. (Canceled).

35. (Currently Amended) The communication device of ~~Claim 1~~claim 20, wherein the processor is in direct data communication with the signal acquisition component.

36.-39. (Cancelled)